REMARKS

Upon entry of the present amendment claim 22 will have been submitted for consideration by the Examiner.

In view of the herein contained remarks, Applicants respectfully request reconsideration and withdrawal of the outstanding rejection set forth in the above-mentioned Official Action together with an indication of the allowability of the claims pending herein. Such action is respectfully requested and is now believed to be appropriate and proper.

In the Official Action, the Examiner has objected to claim 14 because of minor informalities. In particular, the Examiner indicates that the use of "first metal electrode" and "second metal electrode" should not be used because these electrodes are not disclosed as being metal.

In response thereto, Applicants assert that the first and second electrodes are metal. In this regard, Applicants direct the Examiner's attention to page 15, last paragraph, of the specification that discloses that a metal electrode film 100 (first metal electrode) and a further metal electrode film 100' (second metal electrode) are deposited in the trench 2.

More specifically, as shown in figure 4b of the present invention, a metal electrode film 100 is deposited by a ALD, ALCVD or CVD method. The first metal electrode layer 100 is provided on the dielectric layer 70 inside the trench 2 as the second conducting capacitor plate. A second metal electrode layer 100' is provided in the upper region of the trench such that the second metal electrode layer is in electrical connection

with the first metal electrode layer 100. The second metal electrode layer is also deposited by a ALD, ALCVD or CVD method.

Thus, Applicants respectfully assert that the above-noted objection to claim 14 is inappropriate because the first and second electrodes are metal.

The Examiner has indicated that claim 14 needs to be clarified with the addition of "by." In response thereto, Applicants note that providing a first metal electrode layer 100 on the dielectric layer 70 inside the trench 2 as a second conducting capacitor plate 100 is distinct from filling a conducting filling material 80 into the trench 2 and etching back the conducting filling material 80 to the upper side of the first conducting capacitor plate 60 as shown in figure 4b. In this regard, adding "by" between the claim recitations of "providing" and "filling" would be inaccurate. Thus, Applicants respectfully assert that the claim objection is inappropriate because providing a first metal electrode layer is distinct from filling material to the upper side of the first conducting capacitor plate.

In the Official Action, the Examiner has rejected claim 14 as being anticipated by U.S. Patent No. 6,251,722 to WEI et al.

Applicants respectfully traverse and assert that the rejection is inappropriate based the remarks contained herein.

The present disclosed invention is directed to a method for producing a trench capacitor, for use in a semiconductor memory cell as shown in, for example, figure 4b. The method includes forming a trench 2 in a semiconductor substrate and providing a first conducting capacitor plate 60 in the trench as well as providing a dielectric layer 70 as a capacitor dielectric on the first conducting capacitor plate 60. Moreover, the method includes forming an isolation collar 5'' in an upper region of the trench 2 providing a first

metal electrode layer 100 on the dielectric layer 70 inside the trench 2 as a second conducting capacitor plate 100. Additionally, the method includes filling a conducting filling material 80 into the trench 2 and etching back the conducting filling material 80 to the upper side of the first conducting capacitor plate 60 as well as providing a second metal electrode layer 100' in the upper region of the trench such that the second metal electrode layer is in electrical connection with the first metal electrode layer 100, wherein at least one of the dielectric layer 70, the first conducting capacitor plate 60, the first metal electrode layer 100 and the second metal electrode layer 100', is applied by one of an ALD, ALCVD, and CVD method.

More specifically, the conduction filling material 80 is filled into the trench 2 and etched back to the upper side of the first conducting capacitor plate 60, not for providing a first electrode layer 100 but for providing a filling material 80 in the lower part of the trench 2 in order to provide a second metal electrode layer 100' in the upper region of the trench 2 on top of the filling material 80.

Contrary to these features of the present invention, the WEI et al. discloses a composition of a second polysilicon layer 361 on dielectric layer 351 inside the trench. In contradiction to claim 14 of the present invention, the second polysilicon layer 361 of WEI et al. is not a metal layer.

The additional metal electrode film 100', which is deposited and anisotropically etched back so that it remains in the upper region of the trench 2 is in electrical connection with the first metal electrode layer 100, as shown in figure 4b for example.

Contrary to this, WEI et al. just describes the deposition of another polysilicon layer 362 for filling the trench 32. This additional polysilicon layer 362 of WEI et al. is

also not a metal electrode layer, unlike the second metal electrode layer 100' of the present invention. Thus, WEI et al. does not disclose providing a first metal electrode layer on the dielectric layer inside the trench as a second conducting capacitor plate; and providing a second metal electrode layer in the upper region of the trench such that the second metal electrode layer is in electrical connection with the first metal electrode layer as recited by claim 14.

Thus, the method for producing a trench capacitor according to present claim 14 of the present invention provides a trench capacitor having a structure of two thin metal electrode layers 100 and 100', which are in electrical connection with each other. This arrangement provides a reduced electrode resistance compared to the trench capacitor of WEI et al.

WEI et al. merely discloses a trench capacitor, which is completely filled with two polysilicon layers 361 and 362. Such an arrangement provides a much higher resistance of the trench capacitor compared to the present invention.

In particular, Applicants respectfully assert that WEI et al. does not disclose or suggest "providing a first metal electrode layer on the dielectric layer inside the trench as a second conducting capacitor plate." Rather, WEI et al. discloses a composition of a "second polysilicon layer 361" of an "upper electrode 36" on the dielectric layer 351. In this regard, the "polysilicon layer 361" in WEI et al. is not disclosed to be a "metal electrode layer".

Additionally, Applicants respectfully assert that WEI et al. does not disclose or suggest "providing a second metal electrode layer in the upper region of the trench such that the second metal electrode layer is in electrical connection with the first metal

electrode layer." In particular, WEI et al. discloses filling the trench 32 by depositing a "third polysilicon layer 362" of the "upper electrode 36" on the "second polysilicon layer 361". However, the "third polysilicon layer 362" is not disclosed to be a "metal electrode layer".

Applicants further submit that it appears that the second and third polysilicon layers in WEI et al. are intentionally not made metallic, in contrast to the explicit recitation of claim 14 in the present invention. Rather, WEI et al. specifically notes the use of a metal (Arsenic) in the ASG layer 51 in forming the n-type impurity diffusion layer 33 of the bottom electrode 40 by diffusion. In contrast, no process involving a metallic element is disclosed or suggested with respect to "the second polysilicon layer 361" or "the third polysilicon layer 362". Applicants further submit that WEI et al. does not provide any motivation to modify the "second polysilicon layer 361" or the "third polysilicon layer 362" in a manner that would obtain the claimed invention.

Furthermore, the presently claimed invention provides advantages and benefits not provided by the invention disclosed in WEI et al. In particular, as disclosed e.g. with respect to the embodiment of FIG. 4, a first metal electrode film 100 is deposited using an ALD, ALCVD or a CVD method. The first metal electrode layer 100 is provided on the dielectric layer 70 inside the trench 2 as a second conducting capacitor plate. A second metal electrode film 100' is deposited and (anisotropically) etched back so that it remains in the upper region of the trench 2 (see the last paragraph of page 15). The second metal electrode layer 100' is provided in the upper region of the trench 2 in electrical connection with the first metal electrode layer 100, as depicted in FIG. 4. The provision of a structure of two thin metal electrode layers 100 and 100' provides a reduced

electrical resistance in comparison to the trench capacitor of WEI et al. In particular, the two polysilicon layers 361 and 362 of WEI et al. would provide a much higher resistance of the trench capacitor, in comparison with the present invention. Therefore, the presently claimed invention provides a significant benefit not achieved in WEI et al.

Accordingly, for each and all of the reasons set forth above, Applicants respectfully traverse the outstanding rejection of claim 14, and request the reconsideration thereof, together with an indication of the allowability of the claim. Reconsideration and withdrawal of the outstanding rejection are respectfully requested and are now believed to be appropriate and proper.

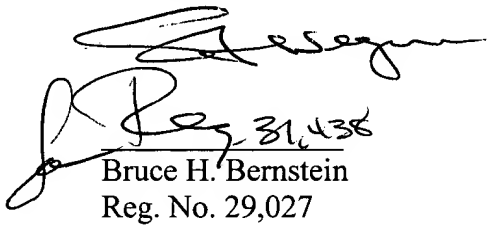
New claim 22 adds no prohibited new matter and is submitted to be allowable. This claim finds support in the specification at, inter alia, figures 4a and 4b. New claim 22 recites additional features that are not disclosed by the prior art.

SUMMARY AND CONCLUSION

Applicants have made a sincere effort to place the present application in condition for allowance and believe that they have now done so. Applicants have pointed out the specific language of Applicant's claims that define over the references of record and respectfully request an indication to such effect, in due course.

Should there be any questions concerning this application, the Examiner is invited to contact the undersigned at the telephone number listed below.

Respectfully submitted,
Harald SEIDL et al.



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